DAC1205D750

Dual 12-bit DAC, up to 750 Msps; 4x and 8x interpolating

Rev. 4 — 31 January 2012

Product data sheet

1. General description

The DAC1205D750 is a high-speed 12-bit dual channel Digital-to-Analog Converter (DAC) with selectable 4× or 8× interpolating filters optimized for multi-carrier wireless transmitters.

Thanks to its digital on-chip modulation, the DAC1205D750 allows the complex I and Q inputs to be converted from BaseBand (BB) to IF. The mixing frequency is adjusted via a Serial Peripheral Interface (SPI) with a 32-bit Numerically Controlled Oscillator (NCO) and the phase is controlled by a 16-bit register.

Two modes of operation are available: separate data ports or a single interleaved high-speed data port. In the Interleaved mode, the input data stream is demultiplexed into its original I and Q data and then latched.

A 4× and 8× clock multiplier enables the DAC1205D750 to provide the appropriate internal clocks from the internal PLL. The internal PLL can be bypassed enabling the use of an external high frequency clock. The voltage regulator enables adjustment of the output full-scale current.

2. Features and benefits

- Dual 12-bit resolution
- 750 Msps maximum update rate
- Selectable 4× or 8× interpolation filters
- Input data rate up to 185 Msps
- Very low noise cap-free integrated PLL
- 32-bit programmable NCO frequency
- Dual port or Interleaved data modes
- 1.8 V and 3.3 V power supplies
- LVDS compatible clock
- Two's complement or binary offset data format
- 1.8 V/3.3 V CMOS input data buffers
- IMD3: 74 dBc; f_s = 737.28 Msps; f_o = 140 MHz
- ACPR: 69 dBc; 2-carrier WCDMA; f_s = 737.28 Msps; f_o = 153.6 MHz
- Typical 1.2 W power dissipation at 4× interpolation, PLL off and 740 Msps
- Power-down and Sleep modes
- Differential scalable output current from 1.6 mA to 22 mA
- On-chip 1.29 V reference
- External analog offset control (10-bit auxiliary DACs)
- Internal digital offset control
- Inverse x / (sin x) function
- Fully compatible SPI port
- Industrial temperature range from –40 °C to +85 °C

3. Applications

- Wireless infrastructure: LTE, WiMAX, GSM, CDMA, WCDMA, TD-SCDMA
- Communication: LMDS/MMDS, point-to-point
- Direct Digital Synthesis (DDS)
- Broadband wireless systems
- Digital radio links
- Instrumentation
- Automated Test Equipment (ATE)

4. Ordering information

Table 1. Ordering information

Type number	**Package**		
	Name	**Description**	**Version**
DAC1205D750HW	HTQFP100	plastic thermal enhanced thin quad flat package; 100 leads; body 14 × 14 × 1 mm; exposed die pad	SOT638-1

5. Block diagram

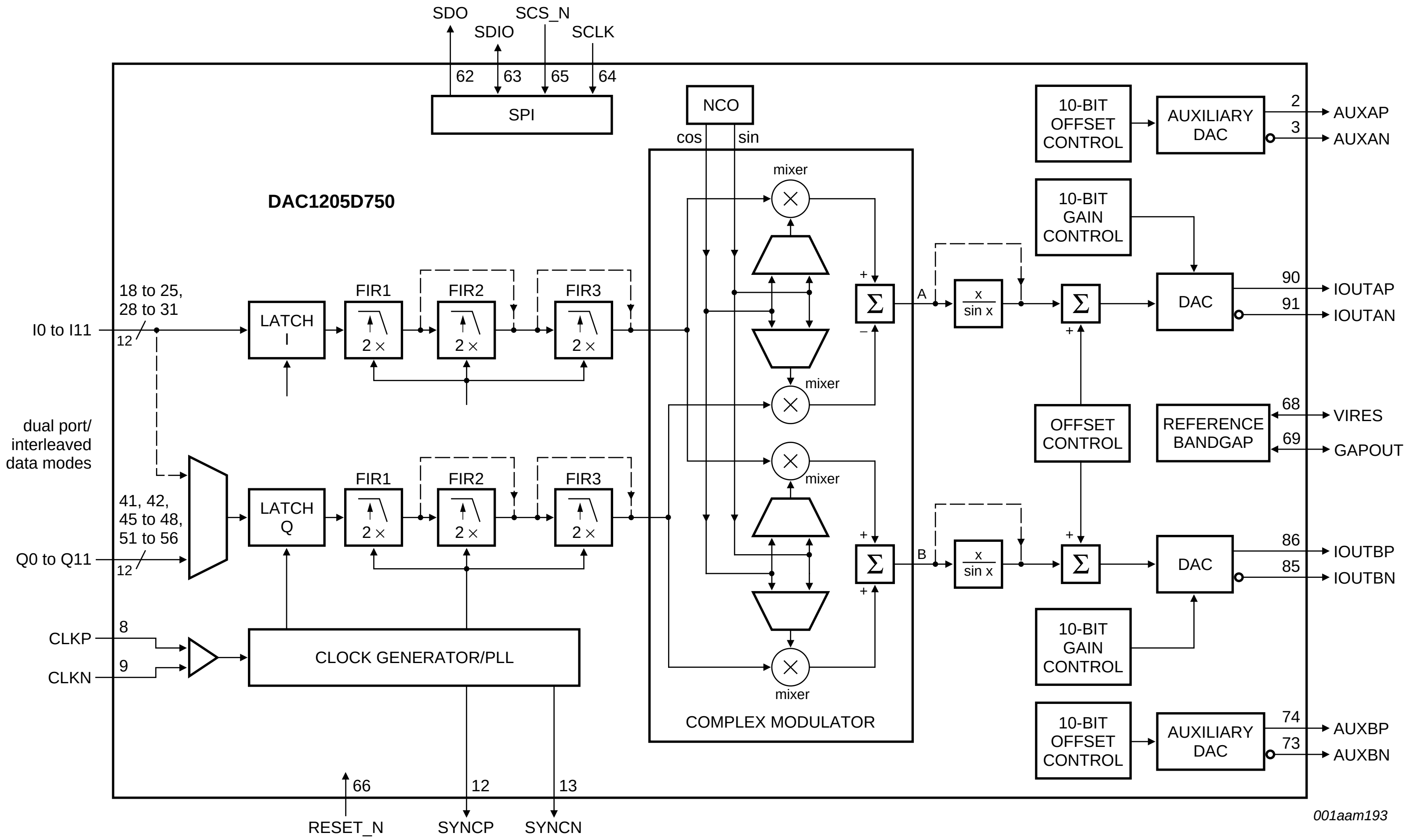


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

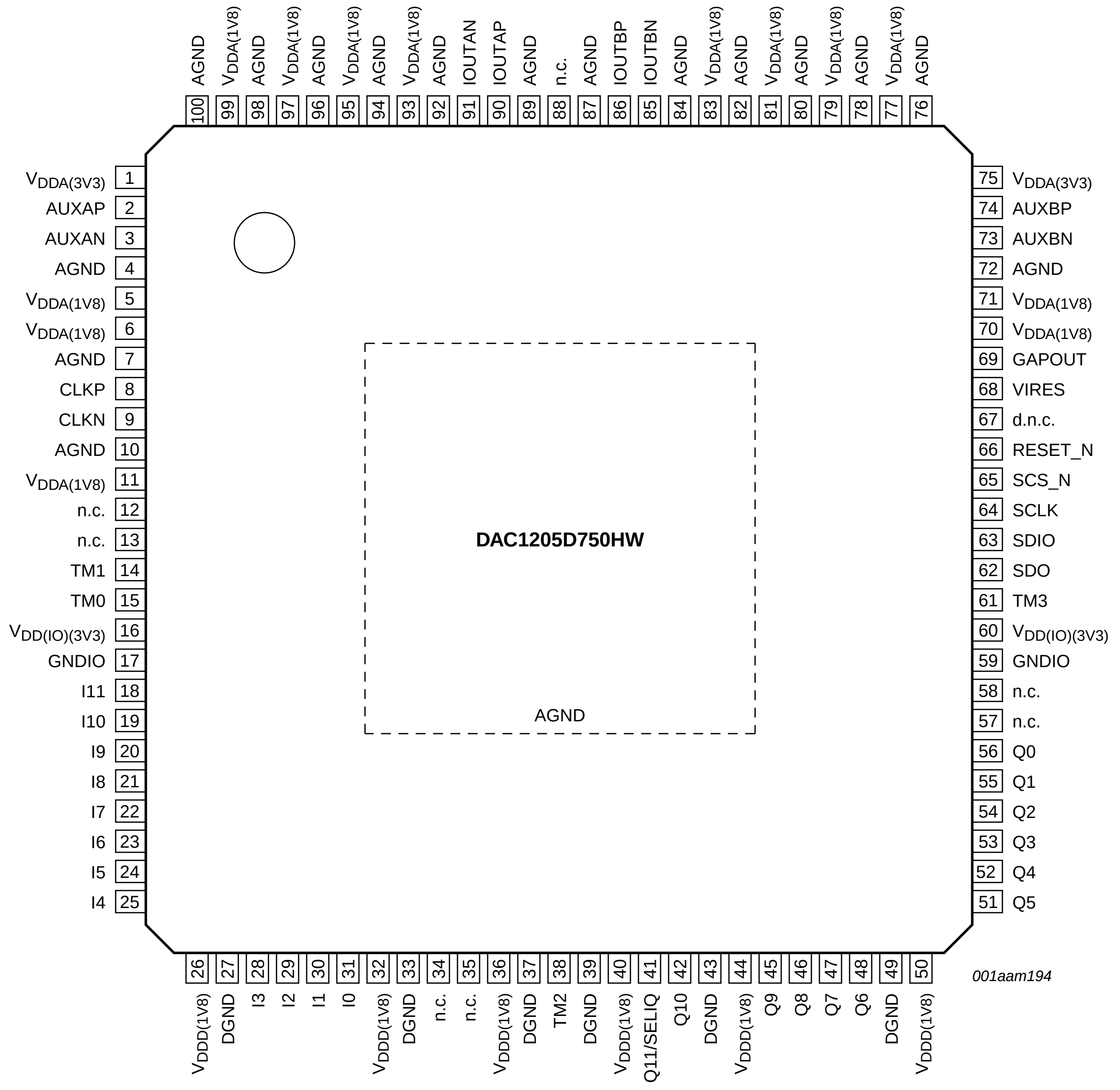


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
$V_{DDA(3V3)}$	1	P	analog supply voltage 3.3 V
AUXAP	2	O	auxiliary DAC B output current
AUXAN	3	O	complementary auxiliary DAC B output current
AGND	4	G	analog ground
$V_{DDA(1V8)}$	5	P	analog supply voltage 1.8 V
$V_{DDA(1V8)}$	6	P	analog supply voltage 1.8 V
AGND	7	G	analog ground
CLKP	8	I	clock input
CLKN	9	I	complementary clock input
AGND	10	G	analog ground
$V_{DDA(1V8)}$	11	P	analog supply voltage 1.8 V
SYNCP	12	O	synchronous clock output
SYNCN	13	O	complementary synchronous clock output
TM1	14	I/O	test mode 1 (connected to DGND)
TM0	15	I/O	test mode 0 (connected to DGND)
$V_{DD(IO)(3V3)}$	16	P	input/output buffers supply voltage 3.3 V
GNDIO	17	G	input/output buffers ground
I11	18	I	I data input bit 11 (MSB)
I10	19	I	I data input bit 10
I9	20	I	I data input bit 9
I8	21	I	I data input bit 8
I7	22	I	I data input bit 7
I6	23	I	I data input bit 6
I5	24	I	I data input bit 5
I4	25	I	I data input bit 4
$V_{DDD(1V8)}$	26	P	digital supply voltage 1.8 V
DGND	27	G	digital ground
I3	28	I	I data input bit 3
I2	29	I	I data input bit 2
I1	30	I	I data input bit 1
I0	31	I	I data input bit 0 (LSB)
$V_{DDD(1V8)}$	32	P	digital supply voltage 1.8 V
DGND	33	G	digital ground
n.c.	34		not connected
n.c.	35		not connected
$V_{DDD(1V8)}$	36	P	digital supply voltage 1.8 V
DGND	37	G	digital ground
TM2	38	-	test mode 2 (to connect to DGND)
DGND	39	G	digital ground

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
$V_{DDD(1V8)}$	40	P	digital supply voltage 1.8 V
Q11/SELIQ	41	I	Q data input bit 11 (MSB)/select IQ in Interleaved mode
Q10	42	I	Q data input bit 10
DGND	43	G	digital ground
$V_{DDD(1V8)}$	44	P	digital supply voltage 1.8 V
Q9	45	I	Q data input bit 9
Q8	46	I	Q data input bit 8
Q7	47	I	Q data input bit 7
Q6	48	I	Q data input bit 6
DGND	49	G	digital ground
$V_{DDD(1V8)}$	50	P	digital supply voltage 1.8 V
Q5	51	I	Q data input bit 5
Q4	52	I	Q data input bit 4
Q3	53	I	Q data input bit 3
Q2	54	I	Q data input bit 2
Q1	55	I	Q data input bit 1
Q0	56	I	Q data input bit 0 (LSB)
n.c.	57	I	not connected
n.c.	58	I	not connected
GNDIO	59	G	input/output buffers ground
$V_{DD(IO)(3V3)}$	60	P	input/output buffers supply voltage 3.3 V
TM3	61	I/O	test mode 3 (to connect to DGND)
SDO	62	O	SPI data output
SDIO	63	I/O	SPI data input/output
SCLK	64	I	SPI clock input
SCS_N	65	I	SPI chip select (active LOW)
RESET_N	66	I	general reset (active LOW)
d.n.c.	67	-	do not connect
VIRES	68	I/O	DAC biasing resistor
GAPOUT	69	I/O	bandgap input/output voltage
$V_{DDA(1V8)}$	70	P	analog supply voltage 1.8 V
$V_{DDA(1V8)}$	71	P	analog supply voltage 1.8 V
AGND	72	G	analog ground
AUXBN	73	O	auxiliary DAC B output current
AUXBP	74	O	complementary auxiliary DAC B output current
$V_{DDA(3V3)}$	75	P	analog supply voltage 3.3 V
AGND	76	G	analog ground
$V_{DDA(1V8)}$	77	P	analog supply voltage 1.8 V
AGND	78	G	analog ground
$V_{DDA(1V8)}$	79	P	analog supply voltage 1.8 V
AGND	80	G	analog ground

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
$V_{DDA(1V8)}$	81	P	analog supply voltage 1.8 V
AGND	82	G	analog ground
$V_{DDA(1V8)}$	83	P	analog supply voltage 1.8 V
AGND	84	G	analog ground
IOUTBN	85	O	complementary DAC B output current
IOUTBP	86	O	DAC B output current
AGND	87	G	analog ground
n.c.	88	-	not connected
AGND	89	G	analog ground
IOUTAP	90	O	DAC A output current
IOUTAN	91	O	complementary DAC A output current
AGND	92	G	analog ground
$V_{DDA(1V8)}$	93	P	analog supply voltage 1.8 V
AGND	94	G	analog ground
$V_{DDA(1V8)}$	95	P	analog supply voltage 1.8 V
AGND	96	G	analog ground
$V_{DDA(1V8)}$	97	P	analog supply voltage 1.8 V
AGND	98	G	analog ground
$V_{DDA(1V8)}$	99	P	analog supply voltage 1.8 V
AGND	100	G	analog ground
AGND	H[2]	G	analog ground

[1] P = power supply
G = ground
I = input
O = output.

[2] H = heatsink (exposed die pad to be soldered)

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(IO)(3V3)}$	input/output supply voltage (3.3 V)		–0.5	+4.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		–0.5	+4.6	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		–0.5	+3.0	V
$V_{DDD(1V8)}$	digital supply voltage (1.8 V)		–0.5	+3.0	V
V_I	input voltage	pins CLKP, CLKN, VIRES and GAPOUT referenced to pin AGND	–0.5	+3.0	V
		pins I11 to I0, Q11 to Q0, SDO, SDIO, SCLK, SCS_N and RESET_N referenced to GNDIO	–0.5	+4.6	V
V_O	output voltage	pins IOUTAP, IOUTAN, IOUTBP, IOUTBN, AUXAP, AUXAN, AUXBP and AUXBN referenced to pin AGND	–0.5	+4.6	V
		pins SYNCP and SYNCN referenced to pin AGND	–0.5	+3.0	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	125	°C

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	19.8	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	[1]	7.7	K/W

[1] In compliance with JEDEC test board, in free air.

9. Characteristics

Table 5. Characteristics

$V_{DDA(1V8)} = V_{DDD(1V8)} = 1.8$ V; $V_{DDA(3V3)} = V_{DD(IO)(3V3)} = 3.3$ V; AGND, DGND and GNDIO shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at T_{amb} = 25 °C; $R_L = 50\ \Omega$ differential; $I_{O(fs)}$ = 20 mA; PLL off unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
$V_{DD(IO)(3V3)}$	input/output supply voltage (3.3 V)		I	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		I	3.0	3.3	3.6	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		I	1.7	1.8	1.9	V
$V_{DDD(1V8)}$	digital supply voltage (1.8 V)		I	1.7	1.8	1.9	V
$I_{DD(IO)(3V3)}$	input/output supply current (3.3 V)	f_o = 19 MHz; f_s = 740 Msps; 4× interpolation; NCO on	I	-	0.5	0.7	mA
$I_{DDA(3V3)}$	analog supply current (3.3 V)	f_o = 19 MHz; f_s = 740 Msps; 4× interpolation; NCO on	I	-	44	50	mA
$I_{DDD(1V8)}$	digital supply current (1.8 V)	f_o = 19 MHz; f_s = 740 Msps; 4× interpolation; NCO on	I	-	181	210	mA
$I_{DDA(1V8)}$	analog supply current (1.8 V)	f_o = 19 MHz; f_s = 740 Msps; 4× interpolation; NCO on	I	-	360	391	mA
I_{DDD}	digital supply current	for x / (sin x) function only	I	-	70	-	mA
P_{tot}	total power dissipation	f_o = 19 MHz; f_s = 740 Msps					
		4× interpolation					
		NCO off; DAC B off	C	-	0.74	-	W
		NCO off	C	-	0.89	-	W
		NCO on; all V_{DD}	C	-	1.12	1.32	W
		8× interpolation					
		NCO on	I	-	1.11	-	W
		Power-down mode:					
		full power-down; all V_{DD}	I	-	0.03	0.06	W
		DAC A and DAC B Sleep mode; NCO on	I	-	0.63	-	W

Table 5. Characteristics *...continued*

$V_{DDA(1V8)} = V_{DDD(1V8)} = 1.8$ V; $V_{DDA(3V3)} = V_{DD(IO)(3V3)} = 3.3$ V; AGND, DGND and GNDIO shorted together; $T_{amb} = -40$ °C to +85 °C; typical values measured at $T_{amb} = 25$ °C; $R_L = 50\ \Omega$ differential; $I_{O(fs)} = 20$ mA; PLL off unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Clock inputs (CLKP and CLKN)[2]							
V_i	input voltage	CLKN $\|V_{gpd}\| < 50$ mV or CLKP	C	[3] 825	-	1575	mV
V_{idth}	input differential threshold voltage	$\|V_{gpd}\| < 50$ mV	C	[3] –100	-	+100	mV
R_i	input resistance		D	-	10	-	MΩ
C_i	input capacitance		D	-	0.5	-	pF
Clock outputs (SYNCP and SYNCN)							
$V_{o(cm)}$	common-mode output voltage		C	-	$V_{DDA(1V8)} - 0.3$	-	V
$V_{O(dif)}$	differential output voltage		C	-	1.2	-	V
R_o	output resistance		D	-	80	-	Ω
Digital inputs (I0 to I11, Q0 to Q11)							
V_{IL}	LOW-level input voltage		C	GNDIO	-	0.8	V
V_{IH}	HIGH-level input voltage		C	1.6	-	$V_{DD(IO)(3V3)}$	V
I_{IL}	LOW-level input current	$V_{IL} = 0.8$ V	I	-	60	-	μA
I_{IH}	HIGH-level input current	$V_{IH} = 2.3$ V	I	-	80	-	μA
Digital inputs (SDO, SDIO, SCLK, SCS_N and RESET_N)							
V_{IL}	LOW-level input voltage		C	GNDIO	-	1.0	V
V_{IH}	HIGH-level input voltage		C	2.3	-	$V_{DD(IO)(3V3)}$	V
I_{IL}	LOW-level input current	$V_{IL} = 1.0$ V	I	-	20	-	nA
I_{IH}	HIGH-level input current	$V_{IH} = 2.3$ V	I	-	20	-	nA
Analog outputs (IOUTAP, IOUTAN, IOUTBP and IOUTBN)							
$I_{O(fs)}$	full-scale output current	register value = 00h	C	-	1.6	-	mA
		default register	C	-	20	-	mA
V_O	output voltage	compliance range	C	1.8	-	$V_{DDA(3V3)}$	V
R_o	output resistance		D	-	250	-	kΩ
C_o	output capacitance		D	-	3	-	pF
ΔE_O	offset error variation		C	-	6	-	ppm/°C
ΔE_G	gain error variation		C	-	18	-	ppm/°C
Reference voltage output (GAPOUT)							
$V_{O(ref)}$	reference output voltage	$T_{amb} = 25$ °C	I	1.24	1.29	1.34	V
$\Delta V_{O(ref)}$	reference output voltage variation		C	-	117	-	ppm/°C
$I_{O(ref)}$	reference output current	external voltage 1.25 V	D	-	40	-	μA
Analog auxiliary outputs (AUXAP, AUXAN, AUXBP and AUXBN)							
$I_{O(aux)}$	auxiliary output current	differential outputs	I	-	2.2	-	mA
$V_{O(aux)}$	auxiliary output voltage	compliance range	C	0	-	2	V
$N_{DAC(aux)mono}$	auxiliary DAC monotonicity	guaranteed	D	-	10	-	bit

Table 5. Characteristics *...continued*

$V_{DDA(1V8)} = V_{DDD(1V8)} = 1.8$ V; $V_{DDA(3V3)} = V_{DD(IO)(3V3)} = 3.3$ V; AGND, DGND and GNDIO shorted together; $T_{amb} = -40$ °C to +85 °C; typical values measured at $T_{amb} = 25$ °C; $R_L = 50\ \Omega$ differential; $I_{O(fs)} = 20$ mA; PLL off unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Input timing (see Figure 10)							
f_{data}	data rate	Dual-port mode input	C	-	-	185	MHz
$t_{w(CLK)}$	CLK pulse width		C	40	-	60	%
$t_{h(i)}$	input hold time		C	1.6	-	-	ns
$t_{su(i)}$	input set-up time		C	0.8	-	-	ns
SYNC signal							
t_d	delay time	$f_{SYNC} = f_s / 4$	C	-	0.21	-	ns
		$f_{SYNC} = f_s / 8$	C	-	0.3	-	ns
		variation	C	-	0.27	-	ps/°C
Output timing							
f_s	sampling frequency		C	-	-	750	Msps
t_s	settling time	to ± 0.5 LSB	D	-	20	-	ns
NCO frequency range							
f_{NCO}	NCO frequency	register values					
		00000000h	D	-	0	-	MHz
		FFFFFFFFh	D	-	740	-	MHz
f_{step}	step frequency		D	-	0.172	-	Hz
Low-power NCO frequency range							
f_{NCO}	NCO frequency	register values					
		00000000h	D	-	0	-	MHz
		F8000000h	D	-	716.875	-	MHz
f_{step}	step frequency		D	-	23.125	-	MHz
Dynamic performance							
SFDR	spurious-free dynamic range	$f_s = 737.28$ Msps					
		$f_{data} = 92.16$ MHz; $B = f_{data} / 2$					
		$f_o = 4$ MHz; 0 dBFS	C	-	77	-	dBc
		$f_{data} = 184.32$ MHz; $B = f_{data} / 2$					
		$f_o = 19$ MHz; 0 dBFS	I	-	74	-	dBc
		$f_o = 70$ MHz; 0 dBFS	C	-	86	-	dBc
$SFDR_{RBW}$	restricted bandwidth spurious-free dynamic range						
		$f_o = 153.6$ MHz; 0 dBFS; $f_{data} = 184.32$ MHz; $f_s = 737.28$ Msps					
		B = 20 MHz	C	-	86	-	dBc
		B = 100 MHz	C	-	80.5	-	dBc
		B = 20 MHz; 8-tone; 500 kHz spacing	C	-	76	-	dBc

Table 5. Characteristics *…continued*

$V_{DDA(1V8)} = V_{DDD(1V8)} = 1.8$ V; $V_{DDA(3V3)} = V_{DD(IO)(3V3)} = 3.3$ V; AGND, DGND and GNDIO shorted together; $T_{amb} = -40$ °C to +85 °C; typical values measured at $T_{amb} = 25$ °C; $R_L = 50\ \Omega$ differential; $I_{O(fs)} = 20$ mA; PLL off unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
IMD3	third-order intermodulation distortion						
		$f_{data} = 184.32$ MHz; $f_s = 737.28$ Msps					
		$f_{o1} = 95$ MHz; $f_{o2} = 97$ MHz	C [4]	-	77	-	dBc
		$f_{o1} = 137$ MHz; $f_{o2} = 143$ MHz	C [4]	-	74	-	dBc
		$f_{o1} = 152.5$ MHz; $f_{o2} = 153.5$ MHz	I [4]	-	74	-	dBc
ACPR	adjacent channel power ratio						
		$f_{data} = 184.32$ MHz; $f_s = 737.28$ Msps; $f_o = 96$ MHz					
		1-carrier; B = 5 MHz	I	-	73	-	dBc
		2-carrier; B = 10 MHz	C	-	70	-	dBc
		4-carrier; B = 20 MHz	C	-	68	-	dBc
		$f_{data} = 184.32$ MHz; $f_s = 737.28$ Msps; $f_o = 153.6$ MHz					
		1-carrier; B = 5 MHz	C	-	72	-	dBc
		2-carrier; B = 10 MHz	C	-	69	-	dBc
		4-carrier; B = 20 MHz	C	-	66.5	-	dBc
NSD	noise spectral density						
		$f_{data} = 184.32$ MHz; $f_s = 737.28$ Msps					
		$f_o = 19$ MHz; 0 dBFS	C	-	−157	-	dBFS/Hz
		$f_o = 153.6$ MHz; 0 dBFS;	C	-	−155	-	dBFS/Hz
		$f_o = 153.6$ MHz; −10 dBFS	C	-	−157	-	dBFS/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] CLKP and CLKN inputs are at differential LVDS levels. An external differential resistor with a value of between 80 Ω and 120 Ω should be connected across the pins (see Figure 8).

[3] $|V_{gpd}|$ represents the ground potential difference voltage. This is the voltage that results from current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground voltages.

[4] IMD3 rejection with −6 dBFS/tone.

10. Application information

10.1 General description

The DAC1205D750 is a dual 12-bit DAC which operates at up to 750 Msps. Each DAC consists of a segmented architecture, comprising a 6-bit thermometer sub-DAC and an 6-bit binary weighted sub-DAC.

The input data rate of up to 185 MHz combined with the maximum output sampling rate of 750 Msps make the DAC1205D750 extremely flexible in wide bandwidth and multi-carrier systems. The device's quadrature modulator and 32-bit NCO simplifies system frequency selection. This is also possible because the 4× and 8× interpolation filters remove undesired images.

A SYNC signal is provided to synchronize data when the PLL is in the off state.

Two modes are available for the digital input. In Dual-port mode, each DAC uses its own data input line. In Interleaved mode, both DACs use the same data input line.

The on-chip PLL enables generation of the internal clock signals for the digital circuitry and the DAC from a low speed clock. The PLL can be bypassed enabling the use of an external, high-speed clock.

Each DAC generates two complementary current outputs on pins IOUTAP/IOUTAN and IOUTBP/IOUTBN. This provides a full-scale output current ($I_{O(fs)}$) up to 22 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

There are also some embedded features to provide an analog offset correction (auxiliary DACs) and digital offset control as well as for gain adjustment. All the functions can be set using the SPI.

The DAC1205D750 operates at both 3.3 V and 1.8 V each of which has separate digital and analog power supplies. The digital input is 1.8 V and 3.3 V compliant and the clock input is LVDS compliant.

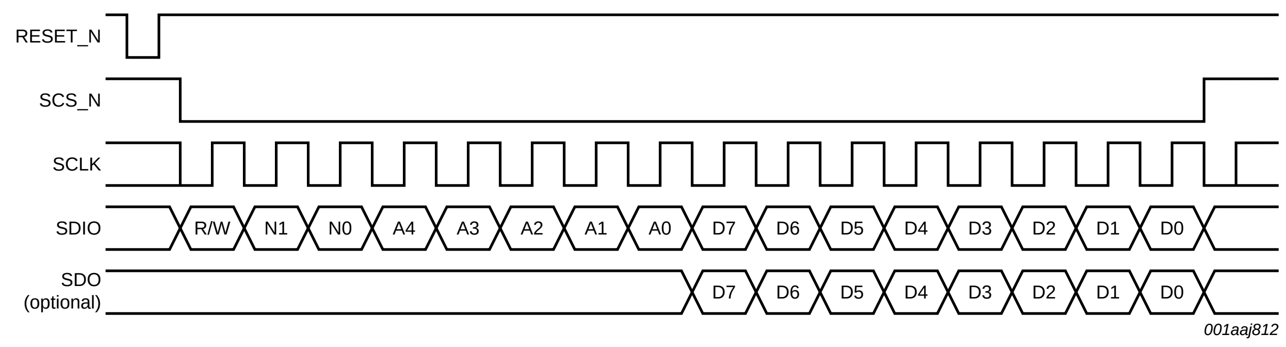
10.2 Serial peripheral interface

10.2.1 Protocol description

The DAC1205D750 Serial Peripheral Interface (SPI) is a synchronous serial communication port allowing easy interfacing with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both write and read modes.

This interface can be configured as a 3-wire type (SDIO as a bidirectional pin) or a 4-wire type (SDIO and SDO as unidirectional pins, input and output port respectively). In both configurations, SCLK acts as the serial clock and SCS_N acts as the serial chip select bar. If several DAC1205D750 devices are connected to an application on the same SPI-bus, only a 3-wire type can be used.

Each read/write operation is sequenced by the SCS_N signal and enabled by a LOW assertion to drive the chip with 1 to 4 bytes, depending on the content of the instruction byte (see Table 7).



R/W indicates the mode access, (see Table 6)

Fig 3. SPI protocol

Table 6. Read or Write mode access description

R/W	Description
0	Write mode operation
1	Read mode operation

In Table 7 N1 and N0 indicate the number of bytes transferred after the instruction byte.

Table 7. Number of bytes transferred

N1	N0	Number of bytes
0	0	1 byte transferred
0	1	2 bytes transferred
1	0	3 bytes transferred
1	1	4 bytes transferred

A0 to A4: indicate which register is being addressed. In the case of a multiple transfer, this address concerns the first register after which the next registers follow directly in a decreasing order according to Table 9 “Register allocation map”.

10.2.2 SPI timing description

The interface can operate at a frequency of up to 15 MHz. The SPI timing is shown in Figure 4.

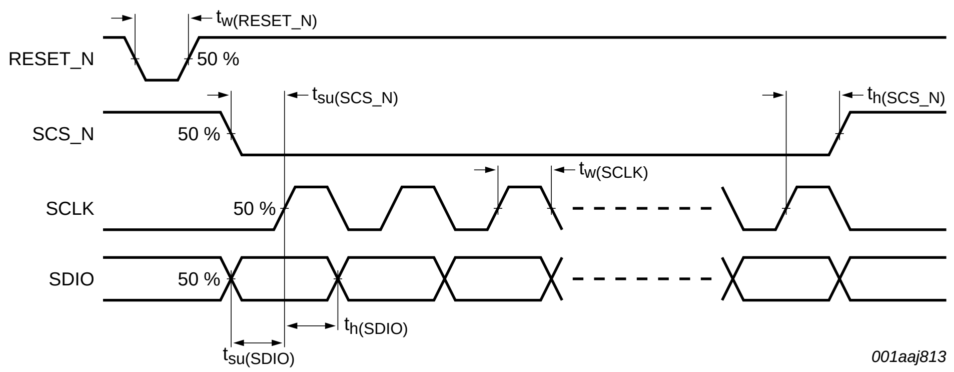


Fig 4. SPI timing diagram

The SPI timing characteristics are given in Table 8.

Table 8. SPI timing characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency	-	-	15	MHz
$t_{w(SCLK)}$	SCLK pulse width	30	-	-	ns
$t_{su(SCS\_N)}$	SCS_N set-up time	20	-	-	ns
$t_{h(SCS\_N)}$	SCS_N hold time	20	-	-	ns
$t_{su(SDIO)}$	SDIO set-up time	10	-	-	ns
$t_{h(SDIO)}$	SDIO hold time	5	-	-	ns
$t_{w(RESET\_N)}$	RESET_N pulse width	30	-	-	ns

10.2.3 Detailed descriptions of registers

An overview of the details for all registers is provided in Table 9.

Table 9. Register allocation map

Address		Register name	R/W	Bit definition								Default		
Dec	Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Dec	Hex
0	00h	COMMon	R/W	3W_SPI	SPI_RST	CLK_SEL	-	MODE_ SEL	CODING	IC_PD	GAP_PD	10000000	128	80
1	01h	TXCFG	R/W	NCO_ON	NCO_LP_ SEL	INV_SIN_ SEL	MODULATION[2:0]			INTERPOLATION[1:0]		10000111	135	87
2	02h	PLLCFG	R/W	PLL_PD	-	PLL_DIV_ PD	PLL_DIV[1:0]		DAC_CLK_DELAY[1:0]		DAC_CLK _POL	00010000	16	10
3	03h	FREQNCO_LSB	R/W	FREQ_NCO[7:0]								01100110	102	66
4	04h	FREQNCO_LISB	R/W	FREQ_NCO[15:8]								01100110	102	66
5	05h	FREQNCO_UISB	R/W	FREQ_NCO[23:16]								01100110	102	66
6	06h	FREQNCO_MSB	R/W	FREQ_NCO[31:24]								00100110	38	26
7	07h	PHINCO_LSB	R/W	PH_NCO[7:0]								00000000	0	00
8	08h	PHINCO_MSB	R/W	PH_NCO[15:8]								00000000	0	00
9	09h	DAC_A_Cfg_1	R/W	DAC_A_PD	DAC_A_ SLEEP	DAC_A_OFFSET[4:0]					-	00000000	0	00
10	0Ah	DAC_A_Cfg_2	R/W	DAC_A_GAIN_ COARSE[1:0]		DAC_A_GAIN_FINE[5:0]						01000000	64	40
11	0Bh	DAC_A_Cfg_3	R/W	DAC_A_GAIN_ COARSE[3:2]		DAC_A_OFFSET[10:5]						11000000	192	C0
12	0Ch	DAC_B_Cfg_1	R/W	DAC_B_PD	DAC_B_ SLEEP	DAC_B_OFFSET[4:0]					-	00000000	0	00
13	0Dh	DAC_B_Cfg_2	R/W	DAC_B_GAIN_ COARSE[1:0]		DAC_B_GAIN_FINE[5:0]						01000000	64	40
14	0Eh	DAC_B_Cfg_3	R/W	DAC_B_GAIN_ COARSE[3:2]		DAC_B_OFFSET[10:5]						11000000	192	C0
15	0Fh	DAC_Cfg	R/W	-						MINUS_ 3DB	NOISE_ SHPER	00000000	0	00
16	10h	SYNC_Cfg	R/W	SYNC_DIV	SYNC_SEL	-						00000000	0	00
26	1Ah	DAC_A_Aux_MSB	R/W	AUX_A[9:2]								10000000	128	80
27	1Bh	DAC_A_Aux_LSB	R/W	AUX_A_PD	-					AUX_A[1:0]		00000000	0	00
28	1Ch	DAC_B_Aux_MSB	R/W	AUX_B[9:2]								10000000	128	80
29	1Dh	DAC_B_Aux_LSB	R/W	AUX_B_PD	-					AUX_B[1:0]		00000000	0	00

10.2.4 Detailed register descriptions

Please refer to Table 9 for the register overview and relevant default values. In the following tables, all the values shown in bold are the default values.

Table 10. COMMon register (address 00h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	3W_SPI	R/W		serial interface bus type
			0	4 wire SPI
			1	**3 wire SPI**
6	SPI_RST	R/W		serial interface reset
			0	**no reset**
			1	performs a reset on all registers except 00h
5	CLK_SEL	R/W		data input latch
			0	**at CLK rising edge**
			1	at CLK falling edge
4	-	-	-	reserved
3	MODE_SEL	R/W		input data mode
			0	**dual port**
			1	interleaved
2	CODING	R/W		coding
			0	**binary**
			1	two’s compliment
1	IC_PD	R/W		power-down
			0	**disabled**
			1	all circuits (digital and analog, except SPI) are switched off
0	GAP_PD	R/W		internal bandgap power-down
			0	**power-down disabled**
			1	internal bandgap references are switched off

Table 11. TXCFG register (address 01h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	NCO_ON	R/W		NCO
			0	disabled (the NCO phase is reset to 0)
			1	**enabled**
6	NCO_LP_SEL	R/W		low-power NCO
			0	**disabled**
			1	NCO frequency and phase given by the five MSBs of the registers 06h and 08h respectively
5	INV_SIN_SEL	R/W		x / (sin x) function
			0	**disabled**
			1	enabled

Table 11. TXCFG register (address 01h) bit description *…continued*

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 2	MODULATION[2:0]	R/W		modulation
			000	dual DAC: no modulation
			001	**positive upper single sideband up-conversion**
			010	positive lower single sideband up-conversion
			011	negative upper single sideband up-conversion
			100	negative lower single sideband up-conversion
1 to 0	INTERPOLATION[1:0]	R/W		interpolation
			01	reserved
			10	4×
			11	**8×**

Table 12. PLLCFG register (address 02h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description	
				PLL ON	PLL OFF
7	PLL_PD	R/W		PLL	
			0	**switched on**	
			1	switched off	
6	-	-	reserved		
5	PLL_DIV_PD	R/W		PLL divider	undefined
			0	**switched on**	**X**
			1	switched off	X
4 to 3	PLL_DIV[1:0]	R/W		PLL divider factor	Digital clock delay
			00	2	130 ps
			01	4	280 ps
			10	**8**	**430 ps**
			11	**X**	580 ps
2 to 1	DAC_CLK_DELAY[1:0]	R/W		phase shift (f_s)	undefined
			00	**0°**	**X**
			01	120°	X
			10	240°	X
0	DAC_CLK_POL	R/W		clock edge of DAC (f_s)	undefined
			0	**normal**	**X**
			1	inverted	X

Table 13. FREQNCO_LSB register (address 03h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[7:0]	R/W	-	lower 8 bits for the NCO frequency setting

Table 14. FREQNCO_LISB register (address 04h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[15:8]	R/W	-	lower intermediate 8 bits for the NCO frequency setting

Table 15. FREQNCO_UISB register (address 05h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[23:16]	R/W	-	upper intermediate 8 bits for the NCO frequency setting

Table 16. FREQNCO_MSB register (address 06h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[31:24]	R/W	-	most significant 8 bits for the NCO frequency setting

Table 17. PHINCO_LSB register (address 07h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PH_NCO[7:0]	R/W	-	lower 8 bits for the NCO phase setting

Table 18. PHINCO_MSB register (address 08h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PH_NCO[15:8]	R/W	-	most significant 8 bits for the NCO phase setting

Table 19. DAC_A_Cfg_1 register (address 09h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	DAC_A_PD	R/W		DAC A power
			0	**on**
			1	off
6	DAC_A_SLEEP	R/W		DAC A Sleep mode
			0	**disabled**
			1	enabled
5 to 1	DAC_A_OFFSET[4:0]	R/W	-	lower 5 bits for the DAC A offset

Table 20. DAC_A_Cfg_2 register (address 0Ah) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_A_GAIN_COARSE[1:0]	R/W	-	lower 2 bits for the DAC A gain setting for coarse adjustment
5 to 0	DAC_A_GAIN_FINE[5:0]	R/W	-	lower 6 bits for the DAC A gain setting for fine adjustment

Table 21. DAC_A_Cfg_3 register (address 0Bh) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_A_GAIN_ COARSE[3:2]	R/W	-	most significant 2 bits for the DAC A gain setting for coarse adjustment
5 to 0	DAC_A_ OFFSET[10:5]	R/W	-	most significant 6 bits for the DAC A offset

Table 22. DAC_B_Cfg_1 register (address 0Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	DAC_B_PD	R/W		DAC B power
			0	**on**
			1	off
6	DAC_B_SLEEP	R/W		DAC B Sleep mode
			0	**disabled**
			1	enabled
5 to 1	DAC_B_OFFSET[4:0]	R/W	-	lower 5bits for the DAC B offset

Table 23. DAC_B_Cfg_2 register (address 0Dh) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_B_GAIN_ COARSE[1:0]	R/W	-	less significant 2 bits for the DAC B gain setting for coarse adjustment
5 to 0	DAC_B_GAIN_ FINE[5:0]	R/W	-	the 6 bits for the DAC B gain setting for fine adjustment

Table 24. DAC_B_Cfg_3 register (address 0Eh) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_B_GAIN_ COARSE[3:2]	R/W	-	most significant 2 bits for the DAC B gain setting for coarse adjustment
5 to 0	DAC_B_ OFFSET[10:5]	R/W	-	most significant 6 bits for the DAC B offset

Table 25. DAC_Cfg register (address 0Fh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	-	-	-	reserved
1	MINUS_3DB	R/W		NCO gain
			0	**unity**
			1	–3 dB
0	NOISE_SHPER	R/W		noise shaper
			0	**disabled**
			1	enabled

Table 26. SYNC_Cfg register (address 10h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SYNC_DIV	R/W		f_s divided by
			0	**4**
			1	8
6	SYNC_SEL	R/W		SYNC selection
			0	**disabled**
			1	enabled
5 to 0	-	-	-	reserved

Table 27. DAC_A_Aux_MSB register (address 1Ah) bit description

Bit	Symbol	Access	Value	Description
7 to 0	AUX_A[9:2]	R/W	-	most significant 8 bits for the auxiliary DAC A

Table 28. DAC_A_Aux_LSB register (address 1Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	AUX_A_PD	R/W		auxiliary DAC A power
			0	**on**
			1	off
6 to 1	-	-		reserved
1 to 0	AUX_A[1:0]	R/W		lower 2 bits for the auxiliary DAC A

Table 29. DAC_B_Aux_MSB register (address 1Ch) bit description

Bit	Symbol	Access	Value	Description
7 to 0	AUX_B[9:2]	R/W	-	most significant 8 bits for the auxiliary DAC B

Table 30. DAC_B_Aux_LSB register (address 1Dh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	AUX_B_PD	R/W		auxiliary DAC B power
			0	**on**
			1	off
6 to 1	-	-		reserved
1 to 0	AUX_B[1:0]	R/W		lower 2-bits for the auxiliary DAC B

10.2.5 Recommended configuration

It is recommended that the following additional settings are used to obtain optimum performance at up to 750 Msps

Table 31. Recommended configuration

Address		Value		
Dec	**Hex**	**Bin**	**Dec**	**Hex**
17	11h	00001010	10	0Ah
19	13h	01101100	**108**	6Ch
20	14h	01101100	108	6Ch

10.3 Input data

The setting applied to MODE_SEL (register 00h[3]; see Table 10 on page 17) defines whether the DAC1205D750 operates in the Dual-port mode or in Interleaved mode (see Table 32).

Table 32. Mode selection

Bit 3 setting	Function	I11 to I0	Q11 to Q0	Pin 41
0	Dual port mode	active	active	Q11
1	Interleaved mode	active	off	SELIQ

10.3.1 Dual-port mode

The data input for Dual-port mode operation is shown in Figure 5 "Dual-port mode". Each DAC has its own independent data input. The data enters the input latch on the rising edge of the internal clock signal and is transferred to the DAC latch.

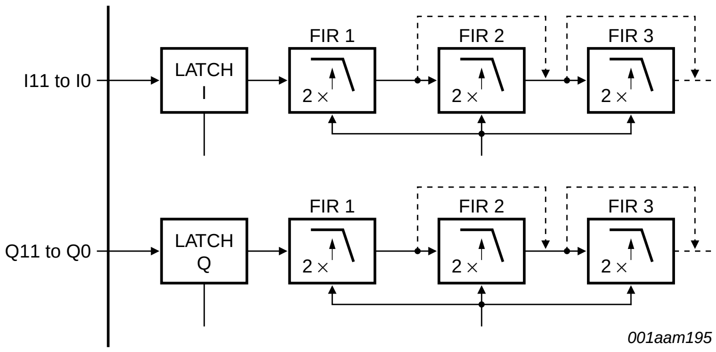


Fig 5. Dual-port mode

10.3.2 Interleaved mode

The data input for the Interleaved mode operation is illustrated in Figure 6 "Interleaved mode operation".

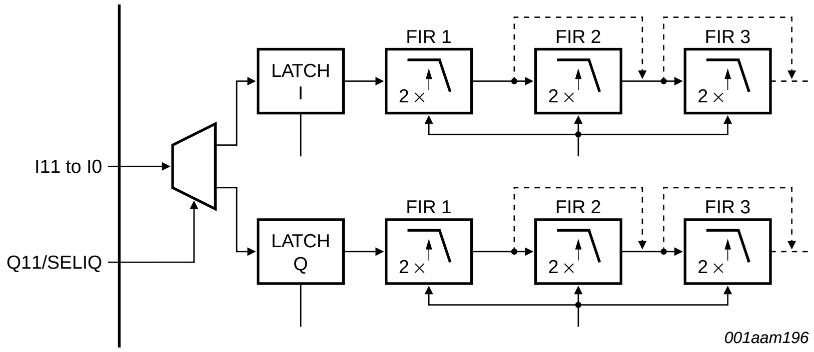
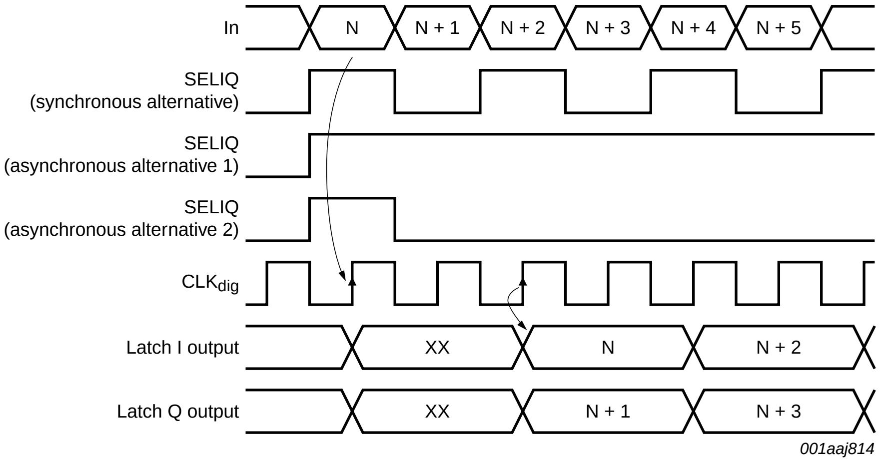


Fig 6. Interleaved mode operation

In Interleaved mode, both DACs use the same data input at twice the Dual-port mode frequency. Data enters the latch on the rising edge of the internal clock signal. The data is sent to either latch I or latch Q, depending on the SELIQ signal.

The SELIQ input (pin 41) allows the synchronization of the internally demultiplexed I and Q channels; see Figure 7.



CLK$_{dig}$ = internal digital clock

Fig 7. Interleaved mode timing (8x interpolation, latch on rising edge)

The SELIQ signal can be either synchronous or asynchronous (single rising edge, single pulse). The first data following the SELIQ rising edge is sent in channel I and following data is sent in channel Q. After this, data is distributed alternately between these channels.

10.4 Input clock

The DAC1205D750 can operate at the following clock frequencies:

PLL on: up to 185 MHz in Dual-port mode and up to 370 MHz in Interleaved mode

PLL off: up to 750 MHz

The input clock is LVDS compliant (see Figure 8) but it can also be interfaced with CML differential sine wave signal (see Figure 9).

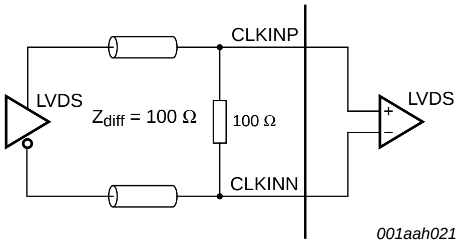


Fig 8. LVDS clock configuration

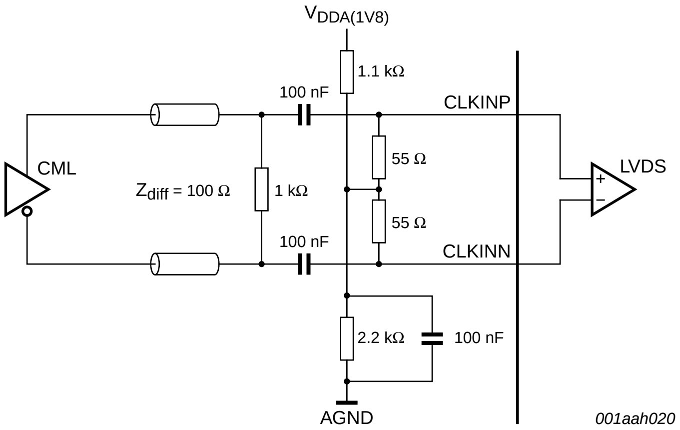


Fig 9. Interfacing CML to LVDS

10.5 Timing

The DAC1205D750 can operate at a sampling frequency (f_s) up to 750 Msps with an input data rate (f_{data}) up to 185 MHz. When using the internal PLL, the input data is referenced to the CLK signal. When the internal PLL is bypassed, the SYNC signal is used as a reference. The input timing in the second case is shown in Figure 10.

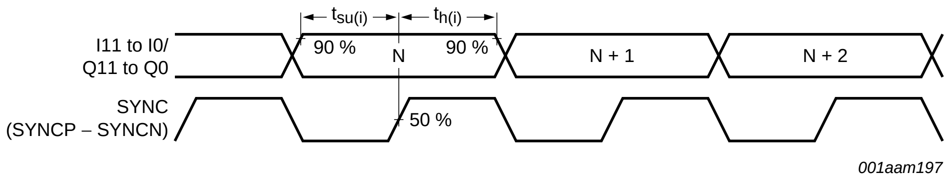


Fig 10. Input timing diagram when internal PLL bypassed (off)

10.5.1 Timing when using the internal PLL (PLL on)

In Table 33, the links between internal and external clocking are defined. The setting applied to PLL_DIV[1:0] (register 02h[4:3]; see Table 9 “Register allocation map”) allows the frequency between the digital part and the DAC core to be adjusted.

Table 33. Frequencies

Mode	CLK input (MHz)	Input data rate (MHz)	Interpolation	Update rate (Msps)	PLL_DIV[1:0]
Dual Port	185	185	4×	740	01 (/ 4)
Dual Port	92.5	92.5	8×	740	10 (/ 8)
Interleaved	370	370	4×	740	00 (/ 2)
Interleaved	185	185	8×	740	01 (/ 4)

The settings applied to DAC_CLK_DELAY[1:0] (register 02h[2:1]) and DAC_CLK_POL (register 02h[0]), allow adjustment of the phase and polarity of the sampling clock. This occurs at the input of the DAC core and depends mainly on the sampling frequency. Some examples are given in Table 34.

Table 34. Sample clock phase and polarity examples

Mode	Input data rate (MHz)	Interpolation	Update rate (Msps)	DAC_CLK_ DELAY [1:0]	DAC_CLK_ POL
Dual Port	92.5	4×	370	01	0
Dual Port	92.5	8×	740	01	0

10.5.2 Timing when using an external PLL (PLL off)

It is recommended that a delay of 280 ps is used on the internal digital clock (CLK_{dig}) to obtain optimum device performance up to750 Msps.

Table 35. Optimum external PLL timing settings

Address		Register name	Value			
Dec	Hex		Digital clock delay	Bin	Dec	Hex
2	02h	PLLCFG	280 ps	10001000	136	88h

10.6 FIR filters

The DAC1205D750 integrates three selectable Finite Impulse Response (FIR) filters which enables the device to use 4× or 8× interpolation rates. All three interpolation filters have a stop-band attenuation of at least 80 dBc and a pass-band ripple of less than 0.0005 dB. The coefficients of the interpolation filters are given in Table 36 “Interpolation filter coefficients”.

Table 36. Interpolation filter coefficients

First interpolation filter			Second interpolation filter			Third interpolation filter		
Lower	**Upper**	**Value**	**Lower**	**Upper**	**Value**	**Lower**	**Upper**	**Value**
H(1)	H(55)	–4	H(1)	H(23)	–2	H(1)	H(15)	–39
H(2)	H(54)	0	H(2)	H(22)	0	H(2)	H(14)	0
H(3)	H(53)	13	H(3)	H(21)	17	H(3)	H(13)	273
H(4)	H(52)	0	H(4)	H(20)	0	H(4)	H(12)	0
H(5)	H(51)	–34	H(5)	H(19)	–75	H(5)	H(11)	–1102
H(6)	H(50)	0	H(6)	H(18)	0	H(6)	H(10)	0
H(7)	H(49)	72	H(7)	H(17)	238	H(7)	H(9)	4964
H(8)	H(48)	0	H(8)	H(16)	0	H(8)	-	8192
H(9)	H(47)	–138	H(9)	H(15)	–660	-	-	-
H(10)	H(46)	0	H(10)	H(14)	0	-	-	-
H(11)	H(45)	245	H(11)	H(13)	2530	-	-	-
H(12)	H(44)	0	H(12)	-	4096	-	-	-
H(13)	H(43)	–408	-	-	-	-	-	-
H(14)	H(42)	0	-	-	-	-	-	-
H(15)	H(41)	650	-	-	-	-	-	-
H(16)	H(40)	0	-	-	-	-	-	-
H(17)	H(39)	–1003	-	-	-	-	-	-
H(18)	H(38)	0	-	-	-	-	-	-
H(19)	H(37)	1521	-	-	-	-	-	-
H(20)	H(36)	0	-	-	-	-	-	-
H(21)	H(35)	–2315	-	-	-	-	-	-
H(22)	H(34)	0	-	-	-	-	-	-
H(23)	H(33)	3671	-	-	-	-	-	-
H(24)	H(32)	0	-	-	-	-	-	-
H(25)	H(31)	–6642	-	-	-	-	-	-
H(26)	H(30)	0	-	-	-	-	-	-
H(27)	H(29)	20756	-	-	-	-	-	-
H(28)		32768	-	-	-	-	-	-

10.7 Quadrature modulator and Numerically Controlled Oscillator (NCO)

The quadrature modulator allows the 12-bit I and Q-data to be mixed with the carrier signal generated by the NCO.

The frequency of the Numerically Controlled Oscillator (NCO) is programmed over 32-bit and allows the sign of the sine component to be inverted in order to operate positive or negative, lower or upper single sideband up-conversion.

10.7.1 NCO in 32-bit

When using the NCO, the frequency can be set by the four registers FREQNCO_LSB, FREQNCO_LISB, FREQNCO_UISB and FREQNCO_MSB over 32 bits.

The frequency for the NCO in 32-bit is calculated as follows:

$$f_{NCO} = \frac{M \times f_s}{2^{32}} \quad (1)$$

where M is the decimal representation of FREQ_NCO[31:0].

The phase of the NCO can be set from 0° to 360° by both registers PHINCO_LSB and PHINCO_MSB over 16 bits.

10.7.2 Low-power NCO

When using the low-power NCO, the frequency can be set by the 5 MSB of register FREQNCO_MSB.

The frequency for the low-power NCO is calculated as follows:

$$f_{NCO} = \frac{M \times f_s}{2^{5}} \quad (2)$$

where M is the decimal representation of FREQ_NCO[31:27].

The phase of the low-power NCO can be set by the 5 MSB of the register PHINCO_MSB.

10.7.3 Minus_3dB function

During normal use, a full-scale pattern will also be full scale at the output of the DAC. Nevertheless, when the I and Q data are simultaneously close to full scale, some clipping can occur and the Minus_3dB function can be used to reduce the gain by 3 dB in the modulator. This is to keep a full-scale range at the output of the DAC without added interferers.

10.8 x / (sin x)

Due to the roll-off effect of the DAC, a selectable FIR filter is inserted to compensate for the x / (sin x) effect. This filter introduces a DC loss of 3.4 dB. The coefficients are represented in Table 37.

Table 37. Inversion filter coefficients

First interpolation filter		
Lower	**Upper**	**Value**
H(1)	H(9)	2
H(2)	H(8)	–4
H(3)	H(7)	10
H(4)	H(6)	–35
H(5)	-	401

10.9 DAC transfer function

The full-scale output current for each DAC is the sum of the two complementary current outputs:

$$I_{O(fs)} = I_{IOUTP} + I_{IOUTN} \tag{3}$$

The output current depends on the digital input data:

$$I_{IOUTP} = I_{O(fs)} \times \left(\frac{DATA}{4095}\right) \tag{4}$$

$$I_{IOUTN} = I_{O(fs)} \times \left(\frac{4095 - DATA}{4095}\right) \tag{5}$$

The setting applied to CODING (register 00h[2]; see Table 9 “Register allocation map”) defines whether the DAC1205D750 operates with a binary input or a two’s complement input.

Table 38 shows the output current as a function of the input data, when $I_{O(fs)}$ = 20 mA.

Table 38. DAC transfer function

Data	I11 to I0 and Q11 to Q0		IOUTP (mA)	IOUTN (mA)
	Binary	Two’s complement		
0	0000 0000 0000	1000 0000 0000	0	20
...	...	...	...	...
8192	1000 0000 0000	0000 0000 0000	10	10
...	...	...	...	...
16383	1111 1111 1111	0111 1111 1111	20	0

10.10 Full-scale current

10.10.1 Regulation

The DAC1205D750 reference circuitry integrates an internal bandgap reference voltage which delivers a 1.29 V reference to the GAPOUT pin. It is recommended to decouple pin GAPOUT using a 100 nF capacitor.

The reference current is generated via an external resistor of 953 Ω (1 %) connected to pin VIRES. A control amplifier sets the appropriate full-scale output current ($I_{O(fs)}$) for both DACs (see Figure 11).

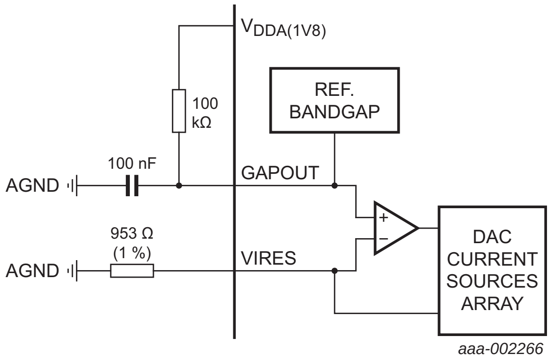


Fig 11. Internal reference configuration

This configuration is optimum for temperature drift compensation because the bandgap reference voltage can be matched to the voltage across the feedback resistor.

The DAC current can also be set by applying an external reference voltage to the non-inverting input pin GAPOUT and disabling the internal bandgap reference voltage with GAP_PD (register 00h[0]; see Table 10 “COMMon register (address 00h) bit description”).

10.10.2 Full-scale current adjustment

The default full-scale current ($I_{O(fs)}$) is 20 mA but further adjustments can be made by the user to both DACs independently via the serial interface from 1.6 mA to 22 mA, ±10 %.

The settings applied to DAC_A_GAIN_COARSE[3:0] (see Table 20 “DAC_A_Cfg_2 register (address 0Ah) bit description” and Table 21 “DAC_A_Cfg_3 register (address 0Bh) bit description”) and to DAC_B_GAIN COARSE[3:0] (see Table 23 “DAC_B_Cfg_2 register (address 0Dh) bit description” and Table 24 “DAC_B_Cfg_3 register (address 0Eh) bit description”) define the coarse variation of the full-scale current (see Table 39).

Table 39. $I_{O(fs)}$ coarse adjustment

Default settings are shown highlighted.

DAC_GAIN_COARSE[3:0]		$I_{O(fs)}$ (mA)
Decimal	Binary	
0	0000	1.6
1	0001	3.0
2	0010	4.4
3	0011	5.8
4	0100	7.2
5	0101	8.6
6	0110	10.0
7	0111	11.4
8	1000	12.8
9	1001	14.2
10	1010	15.6
11	1011	17.0

Table 39. $I_{O(fs)}$ coarse adjustment *…continued*

Default settings are shown highlighted.

DAC_GAIN_COARSE[3:0]		$I_{O(fs)}$ (mA)
Decimal	**Binary**	
12	1100	18.5
13	**1101**	**20.0**
14	1110	21.0
15	1111	22.0

The settings applied to DAC_A_GAIN_FINE[5:0] (see Table 20 “DAC_A_Cfg_2 register (address 0Ah) bit description”) and to DAC_B_GAIN_FINE[5:0] (see Table 23 “DAC_B_Cfg_2 register (address 0Dh) bit description”) define the fine variation of the full-scale current (see Table 40).

Table 40. $I_{O(fs)}$ fine adjustment

Default settings are shown highlighted.

DAC_GAIN_FINE[5:0]		Delta $I_{O(fs)}$
Decimal	**Two’s complement**	
–32	10 0000	–10.3 %
...	...	...
0	**00 0000**	**0**
...	...	...
31	01 1111	+10 %

The coding of the fine gain adjustment is two’s complement.

10.11 Digital offset adjustment

When the DAC1205D750 analog output is DC connected to the next stage, the digital offset correction can be used to adjust the common-mode level at the output of the DAC. It adds an offset at the end of the digital part, just before the DAC.

The settings applied to DAC_A_OFFSET[11:0] (see Table 19 “DAC_A_Cfg_1 register (address 09h) bit description” and Table 21 “DAC_A_Cfg_3 register (address 0Bh) bit description”) and to “DAC_B_OFFSET[11:0]” (see Table 22 “DAC_B_Cfg_1 register (address 0Ch) bit description” and Table 24 “DAC_B_Cfg_3 register (address 0Eh) bit description”) define the range of variation of the digital offset (see Table 41).

Table 41. Digital offset adjustment

Default settings are shown highlighted.

DAC_OFFSET[11:0]		Offset applied
Decimal	**Two's complement**	
–1024	100 0000 0000	–1024
–1023	100 0000 0001	–1023
...	...	...
–1	111 1111 1111	–1
0	**000 0000 0000**	**0**
+1	000 0000 0001	+1
...	...	...
+1022	011 1111 1110	+1022
+1023	011 1111 1111	+1023

10.12 Analog output

The DAC1205D750 has two output channels each of which produces two complementary current outputs. These allow the even-order harmonics and noise to be reduced. The pins are IOUTAP/IOUTAN and IOUTBP/IOUTBN, respectively and need to be connected via a load resistor R_L to the 3.3 V analog power supply ($V_{DDA(3V3)}$).

Refer to Figure 12 for the equivalent analog output circuit of one DAC. This circuit consists of a parallel combination of NMOS current sources, and their associated switches, for each segment.

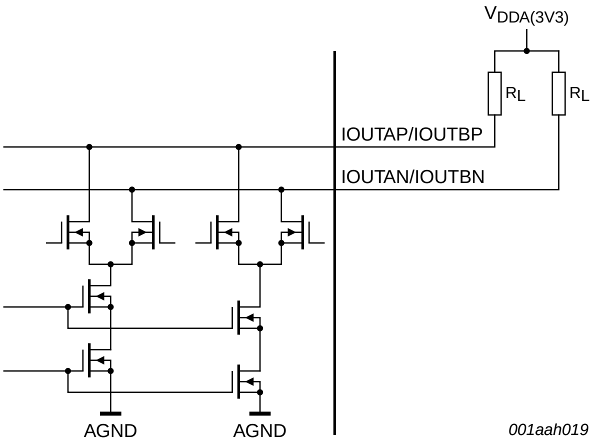


Fig 12. Equivalent analog output circuit (one DAC)

The cascode source configuration increases the output impedance of the source, thus improving the dynamic performance of the DAC by introducing less distortion.

The device can provide an output level of up to 2 $V_{o(p-p)}$ depending on the application, the following stages and the targeted performances.

10.13 Auxiliary DACs

The DAC1205D750 integrates 2 auxiliary DACs that can be used to compensate for any offset between the DAC and the next stage in the transmission path.

Both auxiliary DACs have a resolution of 10-bit and are current sources (referenced to ground).

$$I_{O(AUX)} = I_{AUXP} + I_{AUXN} \quad (6)$$

The output current depends on the auxiliary DAC data:

$$AUXP = I_{O(AUX)} \times \left(\frac{AUX[9:0]}{1023}\right) \quad (7)$$

$$AUXN = I_{O(AUX)} \times \left(\frac{(1023 - AUX[9:0])}{1023}\right) \quad (8)$$

Table 42 shows the output current as a function of the auxiliary DAC data.

Table 42. Auxiliary DAC transfer function

Default settings are shown highlighted.

Data	AUX[9:0] (binary)	I_{AUXP} (mA)	I_{AUXN} (mA)
0	00 0000 0000	0	2.2
...	...	...	...
512	**10 0000 0000**	**1.1**	**1.1**
...	...	...	...
1023	11 1111 1111	2.2	0

10.14 Output configuration

10.14.1 Basic output configuration

The use of a differentially-coupled transformer output provides optimum distortion performance (see Figure 13). In addition, it helps to match the impedance and provides electrical isolation.

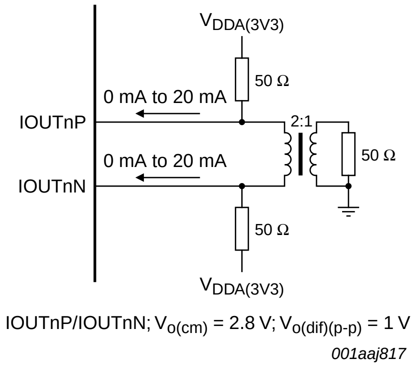
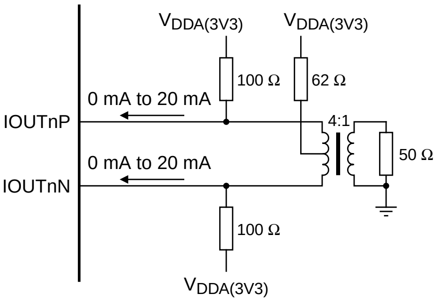


Fig 13. 1 $V_{o(p-p)}$ differential output with transformer

The DAC1205D750 differential outputs can operate up to 2 $V_{o(p-p)}$. In this configuration, it is recommended to connect the center tap of the transformer to a 62 Ω resistor connected to the 3.3 V analog power supply, in order to adjust the DC common-mode to approximately 2.7 V (see Figure 14).



IOUTnP/IOUTnN; $V_{o(cm)}$ = 2.7 V; $V_{o(dif)(p-p)}$ = 2 V

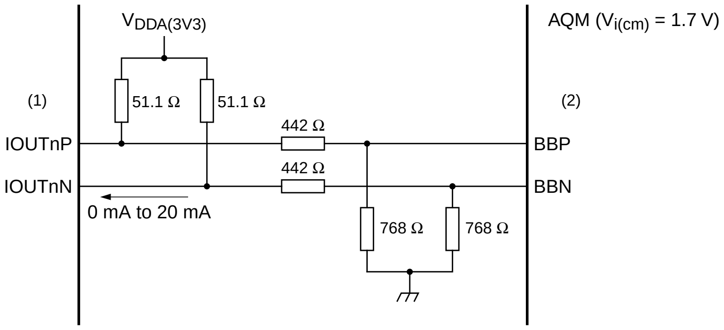
001aaj818

Fig 14. 2 $V_{o(p-p)}$ differential output with transformer

10.14.2 DC interface to an Analog Quadrature Modulator (AQM)

When the system operation requires to keep the DC component of the spectrum, the DAC1205D750 can use a DC interface to connect to an AQM. In this case, the offset compensation for LO cancellation can be made with the use of the digital offset control in the DAC.

Figure 15 provides an example of a connection to an AQM with a 1.7 $V_{I(cm)}$ common-mode input level.



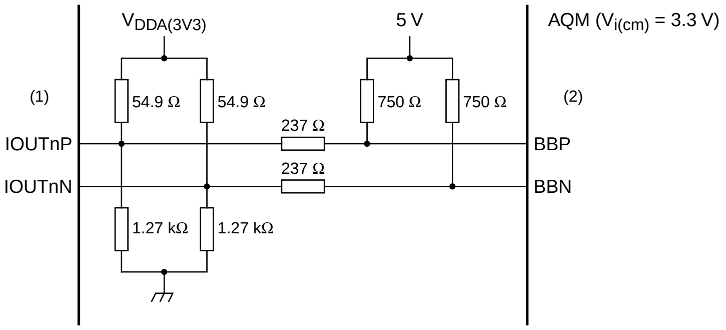
(1) IOUTnP/IOUTnN; $V_{o(cm)}$ = 2.67 V; $V_{o(dif)(p-p)}$ = 1.98 V

(2) BBP/BBN; $V_{i(cm)}$ = 1.7 V; $V_{i(dif)(p-p)}$ = 1.26 V

001aaj541

Fig 15. An example of a DC interface to a 1.7 $V_{I(cm)}$ AQM

Figure 16 provides an example of a connection to an AQM with a 3.3 $V_{I(cm)}$ common-mode input level.



(1) IOUTnP/IOUTnN; $V_{o(cm)}$ = 2.75 V; $V_{o(dif)(p-p)}$ = 1.97 V

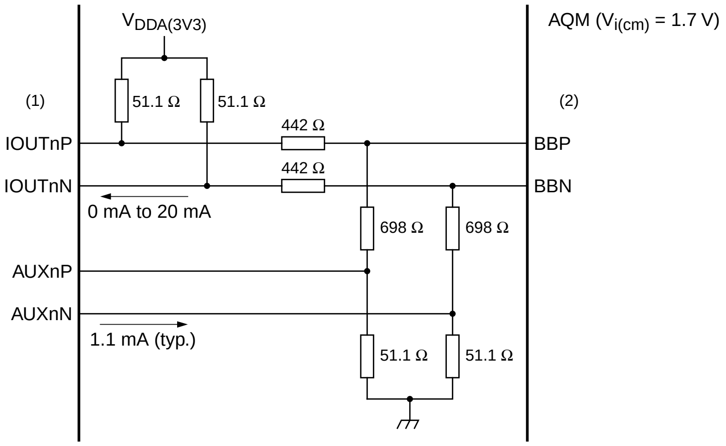
(2) BBP/BBN; $V_{i(cm)}$ = 3.3 V; $V_{i(dif)(p-p)}$ = 1.5 V

001aaj542

Fig 16. An example of a DC interface to a 3.3 $V_{I(cm)}$ AQM

The auxiliary DACs can be used to control the offset in a precise range or with precise steps.

Figure 17 provides an example of a DC interface with the auxiliary DACs to an AQM with a 1.7 $V_{I(cm)}$ common-mode input level.



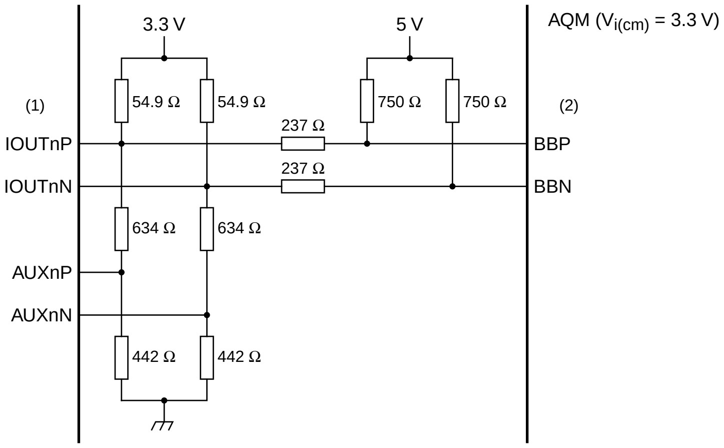
(1) IOUTnP/IOUTnN; $V_{o(cm)}$ = 2.67 V; $V_{o(dif)(p-p)}$ = 1.94 V

(2) BBP/BBN; $V_{i(cm)}$ = 1.7 V; $V_{i(dif)(p-p)}$ = 1.23 V; offset correction up to 50 mV

001aal655

Fig 17. An example of a DC interface to a 1.7 $V_{I(cm)}$ AQM using auxiliary DACs

Figure 18 provides an example of a DC interface with the auxiliary DACs to an AQM with a 3.3 $V_{I(cm)}$ common-mode input level.



(1) IOUTnP/IOUTnN; $V_{o(cm)}$ = 2.75 V; $V_{o(dif)(p-p)}$ = 1.96 V

(2) BBP/BBN; $V_{i(cm)}$ = 3.3 V; $V_{i(dif)(p-p)}$ = 1.5 V; offset correction up to 36 mV

001aaj544

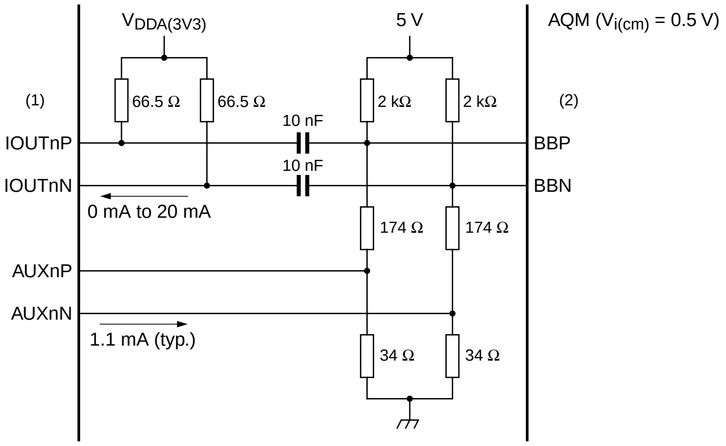
Fig 18. An example of a DC interface to a 3.3 $V_{I(cm)}$ AQM using auxiliary DACs

The constraints to adjust the interface are the output compliance range of the DAC and the auxiliary DACs, the input common-mode level of the AQM, and the range of offset correction.

10.14.3 AC interface to an Analog Quadrature Modulator (AQM)

When the AQM common-mode voltage is close to ground, the DAC1205D750 must be AC-coupled and the auxiliary DACs are needed for offset correction.

Figure 19 provides an example of a connection to an AQM with a 0.5 $V_{I(cm)}$ common-mode input level using auxiliary DACs.



(1) IOUTnP/IOUTnN; $V_{o(cm)}$ = 2.65 V; $V_{o(dif)(p-p)}$ = 1.96 V

(2) BBP/BBN; $V_{i(cm)}$ = 0.5 V; $V_{i(dif)(p-p)}$ = 1.96 V; offset correction up to 70 mV

001aaj589

Fig 19. An example of an AC interface to a 0.5 $V_{I(cm)}$ AQM using auxiliary DACs

10.15 Power and grounding

In order to obtain optimum performance, it is recommended that the 1.8 V analog power supplies on pins 5, 11, 71, 77 and 99 should not be connected with the ones on pins 6, 70, 79, 81, 83, 93, 95 and 97 on the top layer.

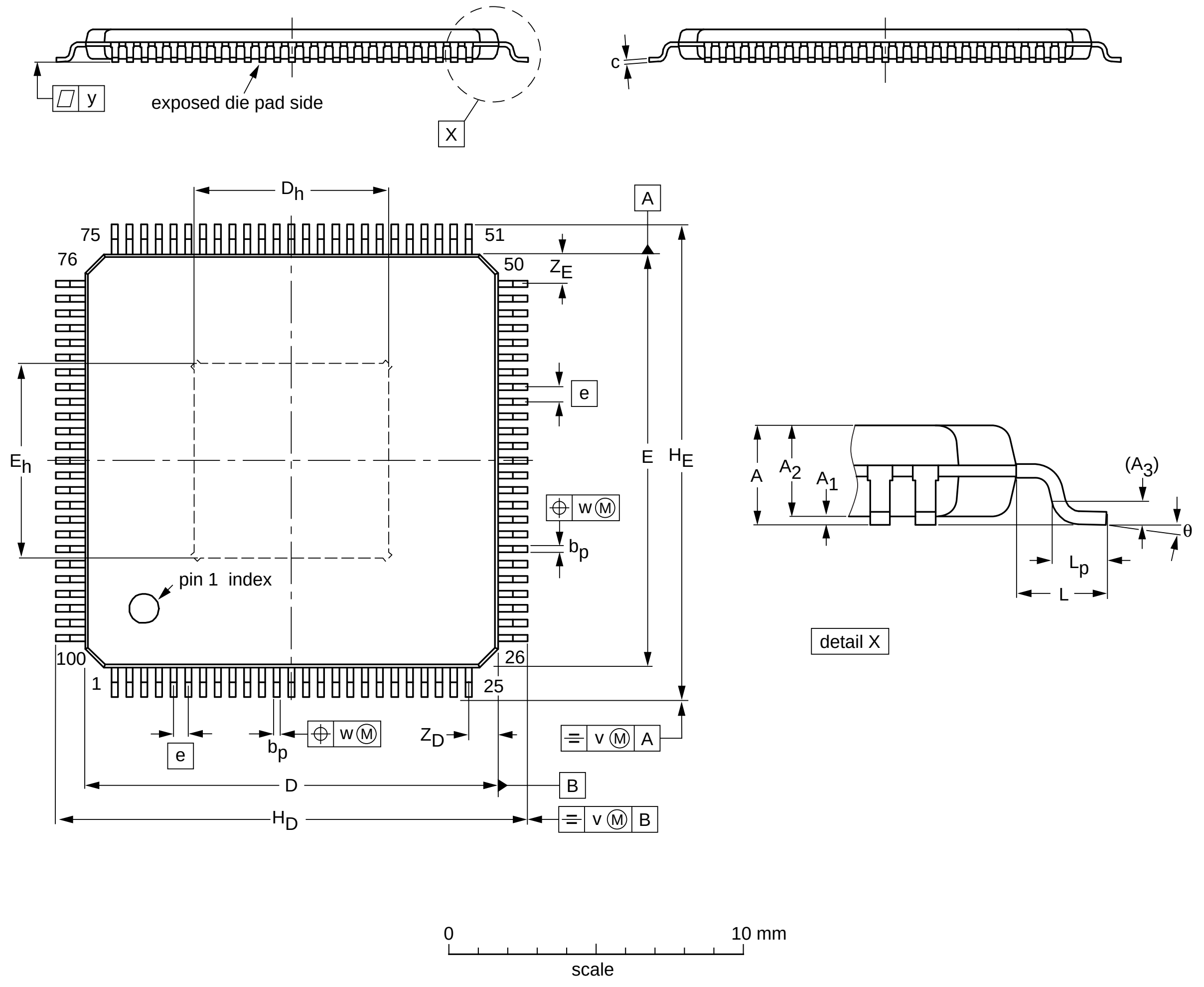
To optimize the decoupling, the power supplies should be decoupled with the following ground pins:

- $V_{DDD(1V8)}$: pin 26 with 27; pin 32 with 33; pin 36 with 37; pin 40 with 39; pin 44 with 43 and pin 50 with 49.
- $V_{DD(IO)(3V3)}$: pin 16 with 17 and pin 60 with 59.
- $V_{DDA(1V8)}$: pin 5 with 4; pin 6 with 7; pin 11 with 10; pin 71 with 72; pin 77 with 78; pins 79, 81, 83 with 80, 82, 84; pins 93, 95, 97 with 92, 94, 96 and pin 99 with 98.
- $V_{DDA(3V3)}$: pin 1 with 100 and pin 75 with 76.

11. Package outline

HTQFP100: plastic thermal enhanced thin quad flat package; 100 leads; body 14 x 14 x 1 mm; exposed die pad

SOT638-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	D_h	E(1)	E_h	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT638-1		MS-026				~~03-04-07~~ 05-02-02

Fig 20. Package outline SOT638-1 (HTQFP100)

12. Abbreviations

Table 43. Abbreviations

Acronym	Description
B	Bandwidth
CDMA	Code Division Multiple Access
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital-to-Analog Converter
FIR	Finite Impulse Response
GSM	Global System for Mobile communications
IF	Intermediate Frequency
IMD3	Third-order InterModulation Distortion
LISB	Lower Intermediate Significant Byte
LMDS	Local Multipoint Distribution Service
LSB	Least Significant Bit
LTE	Long Term Evolution
LVDS	Low-Voltage Differential Signaling
MMDS	Multichannel Multipoint Distribution Service
MSB	Most Significant Bit
NCO	Numerically Controlled Oscillator
NMOS	Negative Metal-Oxide Semiconductor
PLL	Phase-Locked Loop
SFDR	Spurious-Free Dynamic Range
SPI	Serial Peripheral Interface
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
UISB	Upper Intermediate Significant Byte
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access

13. Glossary

Spurious-Free Dynamic Range (SFDR): — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the largest spurious observed (harmonic and non-harmonic, excluding DC component) in the frequency domain.

Intermodulation Distortion (IMD): — From a dual-tone digital input sine wave (these two frequencies being close together), the intermodulation distortion products IMD2 and IMD3 (respectively, second and third-order components) are defined below.

IMD2 — The ratio of the RMS value of either tone to the RMS value of the worst second order intermodulation product.

IMD3 — The ratio of the RMS value of either tone to the RMS value of the worst third order intermodulation product.

Restricted Bandwidth Spurious Free Dynamic Range — The ratio of the RMS value of the reconstructed output sine wave to the RMS value of the noise, including the harmonics, in a given bandwidth centered around f_{offset}.

14. Revision history

Table 44. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
DAC1205D750 v.4	20120131	Product data sheet	-	DAC1205D750 v.3
Modifications:	• Section 2 “Features and benefits” has been updated. • The values for $V_{O(ref)}$ in Table 5 “Characteristics” have been updated. • Section 10.2.1 “Protocol description” has been updated. • Section 10.10.1 “Regulation” has been updated.			
DAC1205D750 v.3	20110607	Product data sheet	-	DAC1205D750 v.2
DAC1205D750 v.2	20100910	Product data sheet	-	DAC1205D750 v.1
DAC1205D750 v.1	20100802	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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